

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

**CLAIMS**

What is claimed is:

Claim 1 (original). A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

- preparing an inter-level dielectric substrate;
- depositing a layer of Ru on the inter-level dielectric substrate;
- depositing a layer of RuO<sub>2</sub> as a diffusion stuffer on the Ru layer; and
- depositing copper on the RuO<sub>2</sub> layer.

Claim 2 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing multiple layers of Ru and RuO<sub>2</sub> between the inter-level dielectric substrate and the copper layer.

Claim 3 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO<sub>2</sub> layer(s) on the Ru layer(s) using an atomic layer deposition technique.

Claim 4 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO<sub>2</sub> layer(s) on the Ru layer(s) using a thermal oxidation technique.

Claim 5 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO<sub>2</sub> layer(s) on the Ru layer(s) using an electrochemical technique.

Claim 6 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO<sub>2</sub> layer(s) on the Ru layer(s) using physical vapor deposition.

Claim 7 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO<sub>2</sub> layer on the Ru layer using an atomic layer deposition technique.

Claim 8 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO<sub>2</sub> layer on the Ru layer using a thermal oxidation technique.

Claim 9 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO<sub>2</sub> layer on the Ru layer using an electrochemical technique.

Claim 10 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO<sub>2</sub> layer on the Ru layer using physical vapor deposition.

Claim 11 (withdrawn). A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

- preparing an inter-level dielectric substrate;
- depositing a layer of Ir on the inter-level dielectric substrate;
- depositing a layer of IrO<sub>2</sub> as a diffusion stuffer on the Ir layer; and
- depositing copper on the IrO<sub>2</sub> layer.

Claim 12 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing multiple layers of Ir and IrO<sub>2</sub> between the inter-level dielectric substrate and the copper layer.

Claim 13 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO<sub>2</sub> layer(s) on the Ir layer(s) using an atomic layer deposition technique.

Claim 14 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO<sub>2</sub> layer(s) on the Ir layer(s) using a thermal oxidation technique.

Claim 15 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO<sub>2</sub> layer(s) on the Ir layer(s) using an electrochemical technique.

Claim 16 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO<sub>2</sub> layer(s) on the Ir layer(s) using physical vapor deposition.

Claim 17 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO<sub>2</sub> layer on the Ir layer using an atomic layer deposition technique.

Claim 18 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO<sub>2</sub> layer on the Ir layer using a thermal oxidation technique.

Claim 19 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO<sub>2</sub> layer on the Ir layer using an electrochemical technique.

Claim 20 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO<sub>2</sub> layer on the Ir layer using physical vapor deposition.

Claim 21 (withdrawn). A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

- preparing an inter-level dielectric substrate;
- depositing a layer of Ir on the inter-level dielectric substrate;
- depositing a layer of RuO<sub>2</sub> as a diffusion stuffer on the Ir layer; and
- depositing copper on the RuO<sub>2</sub> layer.

Claim 22 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 21, further comprising depositing multiple layers of Ir and RuO<sub>2</sub> between the inter-level dielectric substrate and the copper layer.

Claim 23 (withdrawn). A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

- preparing an inter-level dielectric substrate;
- depositing a layer of Ru on the inter-level dielectric substrate;
- depositing a layer of IrO<sub>2</sub> as a diffusion stuffer on the Ru layer; and
- depositing copper on the IrO<sub>2</sub> layer.

Claim 24 (withdrawn). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 21, further comprising depositing multiple layers of Ru and IrO<sub>2</sub> between the inter-level dielectric substrate and the copper layer.

Claim 25 (original). A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

- preparing an inter-level dielectric substrate;
- depositing one or a plurality of layers of RuO<sub>2</sub> on the inter-level dielectric substrate; and
- depositing copper on the RuO<sub>2</sub> layer.

Claim 26 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 25, further comprising depositing the RuO<sub>2</sub> layer on the inter-level dielectric using an atomic layer technique.

Claim 27 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during fabrication of integrated circuits of Claim 25, further comprising depositing the RuO<sub>2</sub> layer on the inter-level dielectric using an electrochemical technique.

Claim 28 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during fabrication of integrated circuits of Claim 25, further comprising depositing the RuO<sub>2</sub> layer on the inter-level dielectric using a thermal oxidation technique.

Claim 29 (original). The method of controlling and containing copper diffusion during the integration of copper interconnects during fabrication of integrated circuits of Claim 25, further comprising depositing the RuO<sub>2</sub> layer on the inter-level dielectric using a physical vapor technique.

Claim 30 (withdrawn). A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing one or a plurality of layers of Ir/Ru on the inter-level dielectric substrate; and

depositing one or a plurality of layers of IrO<sub>2</sub>/RuO<sub>2</sub> on the Ir/Ru layers; and

depositing copper on the IrO<sub>2</sub>/RuO<sub>2</sub> layers.

Claim 31 (original). A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru as a diffusion barrier.

Claim 32 (original). The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 31, further comprising eliminating a copper seed layer.

Claim 33 (original). A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru and RuO<sub>2</sub> as a diffusion barrier.

Claim 34 (original). The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 33, further comprising eliminating a copper seed layer.

Claim 35 (withdrawn). A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ir as a diffusion barrier.

Claim 36 (withdrawn). The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 35, further comprising eliminating a copper seed layer.

Claim 37 (withdrawn). A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ir and IrO<sub>2</sub> as a diffusion barrier.



Claim 38 (withdrawn). The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 37, further comprising eliminating a copper seed layer.

Claim 39 (withdrawn). An integrated circuit, comprising:  
a plurality of semiconductor devices;  
the plurality of semiconductor devices being coupled via copper interconnects;  
the copper interconnects being deposited on one or a plurality of Ru layer(s);  
the Ru layer(s) being deposited on one or a plurality of RuO<sub>2</sub> layer(s); and  
the RuO<sub>2</sub> layer(s) being deposited on an inter-level dielectric.

Claim 40 (withdrawn). The integrated circuit of Claim 39, further comprising the semiconductor devices and copper interconnects having sub-micron features.

Claim 41 (withdrawn). An integrated circuit, comprising:  
a plurality of semiconductor devices;  
the plurality of semiconductor devices being coupled via copper interconnects;  
the copper interconnects being deposited on one or a plurality of Ir layer(s);  
the Ir layer(s) being deposited on one or a plurality of IrO<sub>2</sub> layer(s); and  
the IrO<sub>2</sub> layer(s) being deposited on an inter-level dielectric.

Claim 42 (withdrawn). The integrated circuit of Claim 41, further comprising the semiconductor devices and copper interconnects having sub-micron features.

Claim 43 (withdrawn). An integrated circuit, comprising:  
a plurality of semiconductor devices;

the plurality of semiconductor devices being coupled via copper interconnects;  
the copper interconnects being deposited on one or a plurality of Ru layer(s);  
the Ru layer(s) being deposited on one or a plurality of IrO<sub>2</sub> layer(s); and  
the IrO<sub>2</sub> layer(s) being deposited on an inter-level dielectric.

Claim 44 (withdrawn).        The integrated circuit of Claim 43, further comprising the semiconductor devices and copper interconnects having sub-micron features.

Claim 45 (withdrawn).        An integrated circuit, comprising:  
a plurality of semiconductor devices;  
the plurality of semiconductor devices being coupled via copper interconnects;  
the copper interconnects being deposited on one or a plurality of Ir layer(s);  
the Ir layer(s) being deposited on one or a plurality of RuO<sub>2</sub> layer(s); and  
the RuO<sub>2</sub> layer(s) being deposited on an inter-level dielectric.

Claim 46 (withdrawn).        The integrated circuit of Claim 45, further comprising the semiconductor devices and copper interconnects having sub-micron features.